In the Abstract:

Applicant respectfully requests that the prior Abstract be deleted and a new Abstract inserted as follows:

A reset signal generating circuit and a nonvolatile ferroelectric memory device using the same are disclosed. The reset signal generating circuit generates a reset signal by using a self-bias circuit regardless of a slope time of a power voltage only when the power voltage rises beyond a predetermined voltage. As a result, the reset signal generating circuit may generate a stable reset signal having excellent operation characteristics at short intervals even when the supply of the power source is repeatedly intercepted. Additionally, the reset signal generation circuit may stabilize generation of control signals for controlling a nonvolatile FeRAM, thereby improving the operation characteristics of the memory device.